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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,889	09/28/2001	Robert A. Lester	COMP:0234 P01-3624	4331

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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 08/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/966,889	LESTER ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 1 and 12 recite the limitation "a unidirectional bus configured to transmit only one signal type associated with the request but not including transmission of the data associated with the request". The specification states "each transaction associated with a particular request is exchanged on a single unidirectional bus" and "each bus 30A-30K has a unique signal associated with it and signals are not shared between buses 30A-30K". However, the specification does not state that the signals associated with a single unidirectional bus cannot be data signals.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the Applicant regards as his invention.

4. Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

5. In reference to Claims 1 and 12, it is unclear how data is transmitted between the processor, the memory, and the cache memory if each of the individual buses of the internal bus controller is configured to transmit only one signal type associated with the request and not data associated with the request.

6. In reference to Claims 1, it is unclear if the enchange of a request and data associated with the request occur between the processor, the main memory, and the cache memory all at once or if it only occurs between two of them at once.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 6, 12, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 5,802,269 to Poisner et al. ("Poisner") and US Patent Application Publication Number 2002/0120878 to Lapidus ("Lapidus").

9. In reference to Claim 1, Poisner teaches a system comprising: a processor (See Figure 2 Number 31); a main memory operably coupled to the processor (See Figure 2 Number 35); a cache memory operably coupled to the processor (See Figure 2 Number 39); and a bridge, which is equivalent to a host controller, coupled between the processor and the main memory (See Figure 2 Number 33) and configured to coordinate the exchange of a request and data associated with the request between the processor, the main memory, and the cache memory (See Column 3 Lines 59-67); the host controller comprising: a memory controller operably coupled to the main memory (See Column 3 Lines 61-63); a processor controller operably coupled to the processor (See Column 3 Lines 64-67); and a coherency controller operably coupled to the cache memory (See Column 3 Lines 61-63). Poisner further teaches that the bridge facilitates communications between the processor, the main memory, and the cache memory (See Column 3 Lines 59-67), and thus it inherently includes an internal bus structure configured to couple each of the memory controller, the processor controller, and the coherency controller to each other. Poisner further teaches sending transactions across the bridge (See Column 3 Lines 64-67), wherein said transactions would inherently be sent in an order, and thus the transactions are ordered transactions. Poisner does not

teach that the ordered transactions each have a unique signal type, and wherein each of the individual buses comprises a unidirectional bus configured to transmit only one signal type associated with the request but not including transmission of the data associated with the request. Lapidus teaches a bus structure having a plurality of unidirectional request signal lines that are separate from the data lines (See Page 3 Paragraph 33). Lapidus further teaches that each of the unidirectional request signal lines transmits only one unique signal type, namely REQUEST IN or REQUEST OUT (See Page 3 Paragraphs 38-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the bridge of Poisner with the unidirectional interconnect buses carrying unique signals of Lapidus, resulting in the invention of Claim 1, in order to minimize loading and timing variations (See Page 3 Paragraph 33 of Lapidus).

10. In reference to Claim 2, Poisner and Lapidus teach the limitations as applied to Claim 1 above. Lapidus further teaches that the buses are point-to-point buses wherein each bus connects only two devices together (See Page 3 Paragraph 33).

11. In reference to Claim 3, Poisner and Lapidus teach the limitations as applied to Claim 2 above. Poisner further teaches that the bridge facilitates communications between the processor and the main memory, (See Column 3 Lines 59-67), and thus it

inherently includes the plurality of individual buses coupled between the memory controller and the processor controller.

12. In reference to Claim 4, Poisner and Lapidus teach the limitations as applied to Claim 2 above. Poisner further teaches that the bridge facilitates communications between the cache memory and the main memory, (See Column 3 Lines 59-67), and thus it inherently includes the plurality of individual buses coupled between the memory controller and the coherency controller.

13. In reference to Claim 5, Poisner and Lapidus teach the limitations as applied to Claim 2 above. Poisner further teaches that the bridge facilitates communications between the processor and the cache memory, (See Column 3 Lines 59-67), and thus it inherently includes the plurality of individual buses coupled between the processor controller and the coherency controller.

14. In reference to Claim 6, Poisner and Lapidus teach the limitations as applied to Claim 1 above. Lapidus further teaches that each signal type corresponds to a single transaction in the particular request operation (See Page 3 Paragraphs 39-41).

15. In reference to Claim 12, Poisner teaches a bridge, which is equivalent to a host controller (See Figure 2 Number 33). Poisner further teaches that the bridge facilitates communications between a processor, a main memory, and a cache memory (See

Column 3 Lines 59-67), and thus it inherently includes an internal bus structure configured to couple each of a memory controller, a processor controller, a the coherency controller to each other. Poisner further teaches sending transactions across the bridge (See Column 3 Lines 64-67), wherein said transactions would inherently be sent in an order, and thus the transactions are ordered transactions. Poisner does not teach that the ordered transactions each have a unique signal type, and wherein each of the individual buses comprises a unidirectional bus configured to transmit only one signal type associated with the request but not including transmission of the data associated with the request. Lapidus teaches a bus structure having a plurality of unidirectional request signal lines that are separate from the data lines (See Page 3 Paragraph 33). Lapidus further teaches that each of the unidirectional request signal lines transmits only one unique signal type, namely REQUEST IN or REQUEST OUT (See Page 3 Paragraphs 38-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the bridge of Poisner with the unidirectional interconnect buses carrying unique signals of Lapidus, resulting in the invention of Claim 12, in order to minimize loading and timing variations (See Page 3 Paragraph 33 of Lapidus).

16. In reference to Claim 13, Poisner and Lapidus teach the limitations as applied to Claim 12 above. Lapidus further teaches the use of point-to-point buses wherein each bus connects only two devices together (See Page 3 Paragraph 33).

17. In reference to Claim 14, Poisner and Lapidus teach the limitations as applied to Claim 13 above. Poisner further teaches that the first controller comprises a processor controller (See Column 3 Lines 64-67).

18. In reference to Claim 15, Poisner and Lapidus teach the limitations as applied to Claim 13 above. Poisner further teaches that the second controller comprises a memory controller (See Column 3 Lines 61-63).

19. In reference to Claim 16, Poisner and Lapidus teach the limitations as applied to Claim 12 above. Lapidus further teaches that each signal type corresponds to a single transaction in the particular request operation (See Page 3 Paragraphs 39-41).

20. Claims 7, 8, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner and Lapidus as applied to Claims 6 and 16 above, and further in view of US Patent Number 6,584, 031 to Hanaoka et al. ("Hanaoka").

21. In reference to Claim 7, Poisner and Lapidus teach the limitations as applied to Claim 6 above. Poisner and Lapidus do not teach that each respective signal type includes an identification tag. Hanaoka teaches the use of a header that provides an identification tag for data communicated across a serial interface (See Figure 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner and Lapidus with the header of Hanaoka, resulting in the invention of Claim 18, in order allow the data to be sent in a well-known packet format that can provide information to the receiver regarding the data as well as provide a cyclic redundancy check of the data to insure proper receipt (See Figure 4 of Hanaoka).

22. In reference to Claim 8, Poisner, Lapidus, and Hanaoka teach the limitations as applied to Claim 7 above. Hanaoka further teaches that the identification tag comprises a source identification, a destination identification, and a priority identification, which is equivalent to a cycle identification (See Figure 4).

23. In reference to Claim 17, Poisner and Lapidus teach the limitations as applied to Claim 16 above. Poisner and Lapidus do not teach that each signal type includes an identification tag. Hanaoka teaches the use of a header that provides an identification tag for data communicated across a serial interface (See Figure 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner and Lapidus with the header of Hanaoka, resulting in the invention of Claim 18, in order allow the data to be sent in a well-known packet format that can provide information to the receiver regarding the data as well as provide a cyclic redundancy check of the data to insure proper receipt (See Figure 4 of Hanaoka).

24. In reference to Claim 18, Poisner, Lapidus, and Hanaoka teach the limitations as applied to Claim 17 above. Hanaoka further teaches that the identification tag comprises a source identification, a destination identification, and a priority identification, which is equivalent to a cycle identification (See Figure 4).

25. Claims 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner, Lapidus, and Hanaoka as applied to Claims 8 and 18 above, and further in view of US Patent Number 6,130,886 to Ketseoglou et al. ("Ketseoglou").

26. In reference to Claim 9, Poisner, Lapidus, and Hanaoka teach the limitations as applied to Claim 8 above. Poisner, Lapidus, and Hanaoka do not teach that the cycle identification comprises a toggle bit configured to free the cycle identification for re-use before each transaction in the request operation is complete. Ketseoglou teaches a correlative ID field that appears in signal messages until the link is dropped and can be changed during a connection, and thus enables reuse of the identification before the operation is complete (See Column 11 Lines 60-62 and Column 13 Lines 57-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner, Lapidus, and Hanaoka with the reusable identification numbers of Ketseoglou, resulting in the invention of Claim 9, in order to allow reuse of the number before the connection is completed (See Column 13 Lines 56-61 of Ketseoglou).

27. In reference to Claim 19, Poisner, Lapidus, and Hanaoka teach the limitations as applied to Claim 18 above. Poisner, Lapidus, and Hanaoka do not teach that the cycle identification comprises a toggle bit configured to free the cycle identification for re-use before each transaction in the request operation is complete. Ketseoglou teaches a correlative ID field that appears in signal messages until the link is dropped and can be changed during a connection, and thus enables reuse of the identification before the operation is complete (See Column 11 Lines 60-62 and Column 13 Lines 57-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner, Lapidus, and Hanaoka with the reusable identification numbers of Ketseoglou, resulting in the invention of Claim 19, in order to allow reuse of the number before the connection is completed (See Column 13 Lines 56-61 of Ketseoglou).

28. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner and Lapidus as applied to Claim 1 above, and further in view of US Patent Number 5,901,281 to Miyao et al. ("Miyao").

29. In reference to Claim 10, Poisner and Lapidus teach the limitations as applied to Claim 1 above. Poisner and Lapidus do not teach that the processor comprises the cache memory. Miyao teaches using a processor that has an internal cache (See Column 3 Lines 24-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Poisner and Lapidus with the processor internal cache of Miyao, resulting in the invention of Claim 10, because recent microprocessors generally contain internal cache memories because of improved integration (See Column 3 Lines 24-27 of Miyao).

30. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner and Lapidus as applied to Claim 1 above, and further in view of US Patent Number 6,587,930 to Deshpande et al. ("Deshpande").

31. In reference to Claim 11, Poisner and Lapidus teach the limitations as applied to Claim 1 above. Poisner and Lapidus do not teach a plurality of processor buses; a plurality of processing units, wherein each processing unit is coupled to a respective one of the plurality of processor buses; and a plurality of processor controllers, each processor controller corresponding to a respective one of the plurality of processor buses, wherein the processor controllers are not directly coupled to each other via the internal bus structure. Deshpande teaches a plurality of processor buses (See Figure 4 Numbers 413 and 414); a plurality of processing units, wherein each processing unit is coupled to a respective one of the plurality of processor buses (See Figure 4 Numbers 411 and 412); a plurality of processor controllers, each processor controller corresponding to a respective one of the plurality of processor buses (See Figure 6),

and wherein the processor controllers are not directly coupled to each other via the internal bus structure (See Figure 6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner and Lapidus with the plurality of processing units, processing buses, and processing controllers of Deshpande, resulting in the invention of Claim 11, in order to increase the speed and reliability of the system by utilizing multiple processors as well as to help maintain cache coherency by preventing read-read deadlocks (See Abstract of Deshpande).

Response to Arguments

32. Applicant's arguments with respect to Claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

33. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

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